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Sir:

Transmitted herewith for filing is the patent application of
Inventor(s): William G. Burroughs and Steven J. Pollock
Title: INTER-DSP SIGNALING IN A MULTIPLE DSP ENVIRONMENT
Enclosed are:

- ☒ 5 sheets of drawing.
- ☒ An assignment of the invention to LUCENT TECHNOLOGIES, INC.
- ☒ A Declaration and Power of Attorney.
- ☒ An Associate Power of Attorney.
- ☐ Information Disclosure Statement w/PTO Form 1449 and copy of _ references.
- ☐ This application claims the benefit of U.S. Provisional Application No. __ filed __.

The filing fee has been calculated as shown below:

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Basic Fee				$345	OR		$ 690
Total Claims	26-20=	6	x $9	$	OR	x $18	$ 108
Indep Claims	4-3=	1	x $39	$	OR	x $78	$ 78
☐ Multiple Dependent Claim Presented			+ $130	$	OR	+ $260	$ 0
			TOTAL	$	OR	TOTAL	$ 876

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  - ☒ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

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Date of Deposit: January 24, 2000

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Kathleen Libby

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INTER-DSP SIGNALING IN A MULTIPLE DSP ENVIRONMENT

FIELD OF THE INVENTION

The present invention relates generally to digital signal processors (DSPs) and, more particularly, to interrupt signaling between one DSP and other DSPs.

BACKGROUND OF THE INVENTION

Advances in very large scale integration have contributed to the current digital signal processors (DSPs). These processors are special purpose microprocessors characterized by architectures and instructions suitable for digital signal processing applications. DSPs are utilized in a number of applications from communications and controls to speech and image processing. Special purpose DSPs, designed for a specific signal processing application, such as for fast fourier transform (FFT) have also emerged.

One such DSP, for example the TMS320C30, supports fixed- and floating-point operations. Features of this processor include 32 bit by 32 bit floating-point multiply operations in one instruction cycle time of 60 nsec. Since a number of instructions, such as load and store, multiply and add, can be performed in parallel in one cycle time, the TMS320C30 can execute a pair of instructions in 30 nsec, allowing for 33.3 MIPS. The TMS320C30 has 2K words of on-chip memory and 16 million words of addressable

memory spaces for program, data and input/output. Specialized instructions are available to make common DSP algorithms, such as filtering and spectral analysis, execute fast and efficiently. Like other microprocessors, the DSP may take advantage of higher level languages, such as C and ADA.

In a system having multiple independent DSPs, it is often necessary to synchronize the bit streams running from one DSP to another DSP, and for one DSP to inform or signal another DSP that a specific event has occurred. For example, each DSP may be processing its own independent task, or processing a subset of a task shared by multiple DSPs. When a DSP completes processing a first subset of the task, the DSP signals the other DSP that the first subset has been completed. The other DSP may then perform a second subset of the task. The processors may also exchange data and status information, so that order-dependent processing may proceed correctly.

FIG. 1 illustrates a conventional approach of signaling from one DSP to another DSP. As shown, processing system 10 includes DSPØ, designated as 12, and DSP1, designated as 14. Dedicated lines are connected between DSPØ and DSP1 for providing the signaling function. For example, output 1 terminal of DSPØ provides signal 1 to interrupt 1 terminal of DSP1. By using signal 1, DSPØ informs DSP1 that a specific event has occurred. Signal 1 appears as an interrupt signal to DSP1. FIG. 1 also shows signal 2 placed on another dedicated line between DSPØ and DSP1 for providing a second interrupt to DSP1.

Only a limited number of output terminals in a DSP are available for signaling another DSP. This is a disadvantage as additional signaling may be needed to signal other DSPs in a system. A need exists, therefore, to provide a means for signaling a processor from another processor without depending on the availability of output terminals. The output terminals may then be used for other purposes.

SUMMARY OF THE INVENTION

To meet this and other needs, and in view of its purposes, the present invention provides a method for synchronizing a first processor with a second processor. The method includes storing in a register parallel bits of data from the first processor, wherein at least one bit of data is a logic ONE. An output signal is formed from the one bit of data in the register. The output signal is sent as an interrupt signal to an interrupt terminal of the second processor for synchronizing the first processor with the second processor. The method may be used with a memory mapped register or an off-core register. The first and second processor may be DSP processors or any other type of processors.

It is understood that the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the invention.

BRIEF DESCRIPTION OF THE DRAWING

The invention is best understood from the following detailed description when read in connection with the accompanying drawing. Included in the drawing are the following figures:

FIG. 1 is a block diagram illustrating a conventional system of signaling from one DSP to another DSP;

FIG. 2 is a block diagram illustrating an exemplary embodiment of an inter-DSP signaling system in accordance with the present invention;

FIG. 3 is a block diagram illustrating another exemplary embodiment of an inter-DSP signaling system in accordance with the present invention;

FIG. 4 is a block diagram illustrating a bi-directional inter-DSP signaling system between multiple DSPs in accordance with the present invention;

FIG. 5 is a block diagram illustrating an exemplary embodiment of inter-DSP signaling using an off-core register implementation in accordance with the present invention;

FIG. 6 is a block diagram showing logic circuitry for converting the off-core register implementation of FIG. 5 to a memory-mapped register implementation in accordance with the present invention; and

FIGS. 7(a)-7(i) are timing diagrams showing the relationship of signals as they appear at various points in the exemplary embodiment of FIG. 5.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to communications between DSP cores that exist on the same physical chip and implemented as blocks on the chip, or as separate standalone devices implemented as discrete components on a board that utilizes discrete DSP chips. The present invention, although described for DSP applications, also relates to any other type of processor, such as a general purpose microprocessor, or a microcontroller, for example.

FIG. 2 is a block diagram of inter-DSP signaling system 20 including DSPØ and DSP1, respectively designated as 22 and 24. Interposed between the two DSPs is signal unit 23. As will be explained in detail, signal unit 23 includes a multi-bit register, external to the DSP, that is mapped into the DSPØ's memory space. Signal unit 23 also includes an edge detector to determine when a logic ONE is set in each bit of the register. Depending on which bit is set in the register, signal unit 23 generates a corresponding output signal from the set of signals (for example, signal 1 - signal 8 shown in FIG. 2). One or more of the output signals generated by signal unit 23 is provided to the interrupt terminals (for example, int_1-int_8 shown in FIG. 2) of DSP1. The output signals may be routed to maskable interrupt input terminals, non-maskable interrupt input terminals, or both types of interrupt terminals.

By writing a logic ONE to a predetermined address of the signal unit, DSPØ may synchronize with DSP1 by generating a maskable or non-maskable interrupt in DSP1. This method may be repeated between any pair of DSPs, permitting any DSP to signal any other DSP in the system. In addition, the output signals may be routed to multiple DSPs, as shown in FIG. 2. Signals 1-8 are shown routed to DSP1; another output signal (not labeled) may be routed to another DSP (not shown). Although a single output signal is shown being routed to other DSPs, there may be another set of eight output signals being routed to the other DSPs. As will be explained, the number of independent output signals is a function of the number of bits in the multi-bit register. For example, if signal unit 23 includes a 16-bit register, 16 independent output signals may be generated and routed to any 16 different interrupt input terminals of one or more DSPs.

It will be appreciated that the dedicated output terminals of DSPØ are available for other functions in system 20. For example, output 1 and output 2 terminals may be used for purposes other than providing interrupt signaling, as shown in FIG. 2.

FIG. 3 illustrates another embodiment of the invention, generally designated as 30. As shown, system 30 includes signal unit 33 generating output signals for DSPØ (designated as 32). DSPØ may synchronize with DSP1 (designated as 34) by using the output signals generated by signal unit 33 (designated as 33).

As will be explained, the inter-DSP signaling of system 30 is similar to the inter-DSP signaling of system 20, except for address decoding. System 30 does not require address decoding, while system 20 requires decoding. The difference in decoding is due to signal unit 23 (FIG. 2) having a memory-mapped register (not shown), while signal unit 33 (FIG. 3) has an off-core register (not shown) that is not accessible in the DSP's address space.

A memory-mapped register exists at a particular address in the DSP's address space. The register receives a full address on bus 25, data on bus 26 and a write/read command on line 27, as shown in FIG. 2. Writing or reading to/from the register in signal unit 23 is similar to writing or reading to/from any other memory location accessible by DSPØ. The logic that performs the memory mapping (shown in FIGS. 4 and 6) decodes the address to determine if the register is being accessed, and the read/write command determines whether data on the data bus is being loaded to the register or data is being driven onto the data bus from the register.

An off-core register is not accessible in the DSP's address space. Dedicated hardware in the DSP directly accesses this type of register. The register is accessed by using read/write strobes from the hardware and compiler support to provide instructions to access the hardware. The address and read/write decoding necessary in memory-mapped register operations is unnecessary for off-core register operations. As shown in FIG. 3 (and in greater detail in FIG. 5), data bus 36 and write strobe line 37 are connected to signal unit 33; the address bus is not used.

Referring to FIG. 4, inter-DSP signaling between multiple DSPs will now be explained in greater detail. As shown, bi-directional inter-DSP signaling system 40 includes multiple DSPs; only two (DSPØ and DSPx) are shown, respectively designated as 41 and 46. Signaling unit Ø, generally designated as 42, forms a set of output signals from data bits having been placed on data bus 81 by DSPØ. The formed output signals are placed on dedicated lines 89 and routed to the interrupt terminals of respective DSPs. For example, one interrupt terminal, designated as 87, is shown in DSPx.

Similarly, signaling unit x, generally designated as 47, forms another set of output signals from data bits having been placed on data bus 84 by DSPx. The output signals are placed on dedicated lines 90 and routed to the interrupt terminals of respective DSPs. For example, one interrupt terminal, designated as 88, is shown in DSPØ.

Data bits on data bus 81 are stored in memory-mapped register 44, after decoder 43 determines that the address placed on address bus 82 matches the address of register 44. Decoder 43 is enabled by a write command on line 83 and register 44 is enabled by an output signal from decoder 43. When data is clocked out from the Q output terminal of register 44, the data is detected by edge detector 45. A logic ONE on any data bit from register 44 provides an output signal on a specific line of dedicated lines 89. The output signal may then be provided as an interrupt signal to any processor, for example, an interrupt signal to interrupt terminal 87 of DSPx.

Similarly, decoder 50 enables memory-mapped register 49, after a write command is placed on line 86 and a correct address is placed on address bus 85. Edge detector 48 detects a logic ONE on any data bit being clocked out from register 49 and provides an output signal on dedicated lines 90. The output signal is routed to any processor for use as an interrupt signal. For example, the output signal may be routed to interrupt terminal 88 of DSPØ, as shown in FIG. 4.

It will be appreciated that data busses 81 and 84 each transmit parallel data bits, for example 16 parallel data bits on 16 parallel lines, respectively. Similarly, registers 44 and 49 each include multiple flip/flops, for example 16 flip/flops, each flip/flop storing one bit of data. Edge detectors 45 and 48 are each capable of detecting a logic ONE from any Q output terminal of the multiple flip/flops of respective registers 44 and 49. Each edge detector may then provide multiple output signals for use as interrupts. For example, if register 44 includes 16 flip/flops, then 16 independent output signals may be provided to multiple processors for use as interrupts.

Operation of the inter-DSP signaling system will now be explained in greater detail by referring to FIGS. 5-7. FIG. 5 depicts a signaling unit, generally designated as 52. The decoder function includes a set of 16 AND-gates 53. The register includes a first set of 16 flip/flops 54 and the edge detector includes a second set of 16 flip/flops 55 and a set of 16 AND-gates 56.

A write strobe (wr_sig) is provided to each AND-gate of the 16 AND-gates 53. Each data bit of data bus (15..0) is also provided to one AND-gate of the 16 AND-gates 53. Each AND-gate 53 is enabled, when the write strobe is a logic ONE and a respective data bit is a logic ONE. A logic ONE is clocked into a respective flip/flop 54 of the register by the clock signal. On the next clock, the data passes from flip/flop 54 into flip/flop 55. An interrupt signal is enabled on one of the output lines (int(15..0)) when a respective Q terminal of flip/flop 54 has a logic ONE and a respective QN (Q-not) terminal of flip/flop 55 has a logic ONE.

The operation of signaling unit 52 may be better understood by referring to FIG. 7. As shown, the input signals to system 52, namely the clock, the data on data bus (15..0) and the write strobe (wr_sig), are illustrated as a function of time, respectively in FIGS. 7(a)-7(c). For example, data bit Ø (LSB) is a logic ONE during the first clock cycle and data bits Ø and 1 are both logic ONE during the third clock cycle, as shown in FIG. 7(b).

The signal provided to the D terminal of each of the first set of 16 flip/flops 54 (the register) is shown in FIG. 7(d). The signal is the same as the signal shown in FIG. 7(b). The output signal from the Q terminal of each of the 16 flip/flops 54 is shown in FIG. 7(e). The output signal is delayed by one clock cycle from the input signal at the D terminals of the register. FIG. 7(f) depicts the output signal from the QN output terminals of the second set of 16 flip/flops 55. The second QN output signal is a logical inverse of the first Q output signal, after it is delayed by one clock cycle.

After logically combining the output signal from the Q output terminals of the register and the output signal from the QN output terminals of the second set of flip/flops 55, AND-gate 56 generates an interrupt signal (int(15..0)), as shown in FIG. 7(g). The first write signal (FIG. 7(c)) sets bit Ø, which causes int(0) to be asserted for one clock cycle, as shown in FIG. 7(h). The second write signal (FIG. 7(c)) sets bits Ø and 1, which causes both int(0) and int(1) to be asserted for one clock cycle, as shown in FIGS. 7(h) and 7(i), respectively.

Register 54, as shown in FIG. 5, is an off-core implementation. To convert register 54 from an off-core implementation to a memory-mapped implementation, the circuitry shown in FIG. 6 may be incorporated into the inter-DSP signaling system of FIG. 5. The wr_sig signal of FIG. 5 is replaced by an address bus, a write/read signal and logic circuitry for comparing the address on the address bus to the address of the register. Circuit 60, which performs the logic, includes comparator 62, constant 61 and AND-gate 63. As shown, when the address on address bus (15..0) matches the address of the register (shown as constant 61) and the write command is set, AND-gate 63 enables the write signal.

The signaling system described herein may be used by any one DSP to synchronize with any other DSP or multiple DSPs by simply writing a logic one to the appropriate bit at the appropriate address. Any register (memory mapped or off-core) may be used by the DSP. Since existing registers are used, it will be appreciated that modifications are not required to existing DSP circuitry. The described method of signaling may be repeated

between any pair of DSPs. The interrupt lines from any DSP may also be connected to any number of other DSPs, enabling one DSP to signal multiple DSPs. Furthermore, the DSPs (or other types of processors) and the signaling unit may be implemented on an integrated circuit (IC).

Although illustrated and described herein with reference to certain specific embodiments, the present invention is nevertheless not intended to be limited to the details shown. Rather, various modifications may be made in the details within the scope and range of equivalents of the claims and without departing from the spirit of the invention. It will be understood, for example, that the present invention is not limited to only the DSP described. Rather, the invention may be extended to be used by any processor or microprocessor.

What is claimed:

1. In a system having first and second processors, a method of synchronizing the first processor with the second processor, comprising the steps of:

(a) storing in a register parallel bits of data from the first processor, wherein at least one bit of data is a logic ONE,

(b) forming an output signal from the at least one bit of data in the register, and

(c) sending the output signal to an interrupt terminal of the second processor for synchronizing the first processor with the second processor.

2. The method of claim 1 wherein the register is a memory mapped register.

3. The method of claim 1 wherein the register is an off-core register.

4. The method of claim 1 wherein at least one of the first and second processors is a digital signal processor (DSP).

5. The method of claim 1 wherein step (b) includes detecting a leading edge of the at least one bit of data to form the output signal.

6. The method of claim 5 wherein step (c) includes sending the output signal on a dedicated line between the register and the interrupt terminal.

7. The method of claim 6 wherein the output signal is active for a duration of a clock period.

8. The method of claim 1 including the steps of

enabling the register during a write cycle, and

storing the parallel bits of data when an address of the register matches a predetermined address.

9. A system for providing an interrupt signal from a first processor to a second processor comprising

a data bus coupled to the first processor for routing parallel bits of data,

a register coupled to the data bus for storing the parallel bits of data, at least one of the parallel bits of data having an active logic level,

an edge detector coupled to the register for detecting active logic levels stored in the register and converting each active logic level into an interrupt signal, and

at least one line coupled between the edge detector and an interrupt terminal of the second processor for routing one of the interrupt signals to the interrupt terminal.

10. The system of claim 9 wherein the register includes a first set of flip/flops, each flip/flop storing one of the active logic levels, and

the edge detector includes a second set of flip/flops, each flip/flop detecting one of the active logic levels.

11. The system of claim 9 further including

an address bus coupled between the first processor and the register, and

a predetermined address for the register,

wherein the first processor routes the parallel bits of data to the register by setting the predetermined address on the address bus.

12. The system of claim 9 wherein the register is an off-core register and is enabled by a write strobe signal from the first processor.

13. The system of claim 9 wherein at least one of the first and second processors is a DSP.

14. In a multi-processor system having data lines between each processor and at least one interrupt terminal in each processor, a system for synchronizing a first processor with a second processor comprising

a register coupled to the data lines for storing data bits from the first processor, each data bit representing an interrupt signal,

a detector for detecting each of the data bits in the register, and

a signal router for routing each of the detected data bits to a respective interrupt terminal in the second processor,

wherein when the first processor stores a data bit in the register, the router provides an interrupt signal to the second processor.

15. The system of claim 14 wherein the register includes a first set of flip/flops, each flip/flop storing one of the data bits, and

the detector includes a second set of flip/flops, each flip/flop detecting one of the data bits in the register.

16. The system of claim 14 wherein the signal router includes a set of lines, each line connected to the respective interrupt terminal.

17. The system of claim 14 wherein at least one processor is a DSP.

18. The system of claim 14 further including an address bus coupled to the register, wherein the data bits are stored in the register when the first processor addresses the register.

19. The system of claim 14 wherein the data bits are stored in the register during a first clock cycle and the data bits are detected by the detector during a second clock cycle, and

the interrupt signal is enabled for a duration of a clock cycle.

20. In an integrated circuit including at least two processors, data lines between each processor, and at least one interrupt terminal in each processor, a system for synchronizing a first processor with a second processor comprising

a register coupled to the data lines for storing data bits from the first processor, each data bit representing an interrupt signal,

a detector for detecting each of the data bits in the register, and

a signal router for routing each of the detected data bits to a respective interrupt terminal in the second processor,

wherein when the first processor stores a data bit in the register, the router provides an interrupt signal to the second processor.

21. The system of claim 20 wherein the register includes a first set of flip/flops, each flip/flop storing one of the data bits, and

the detector includes a second set of flip/flops, each flip/flop detecting one of the data bits in the register.

22. The system of claim 20 wherein the signal router includes a set of lines, each line connected to the respective interrupt terminal.

23. The system of claim 20 wherein at least one processor is a DSP.

24. The system of claim 20 wherein at least one processor is a microprocessor.

25. The system of claim 20 further including an address bus coupled to the register, wherein the data bits are stored in the register when the first processor addresses the register.

26. The system of claim 20 wherein the data bits are stored in the register during a first clock cycle and the data bits are detected by the detector during a second clock cycle, and

the interrupt signal is enabled for a duration of a clock cycle.

ABSTRACT

The invention includes a method and apparatus for synchronizing a first processor with a second processor. The method includes storing in a register parallel bits of data from the first processor, wherein at least one bit of data is a logic ONE. An output signal is formed from the one bit of data in the register. The output signal is sent as an interrupt signal to an interrupt terminal of the second processor for synchronizing the first processor with the second processor. The method may be used with a memory mapped register or an off-core register. The first and second processors may each be a digital signal processor (DSP) or any other type of processor.

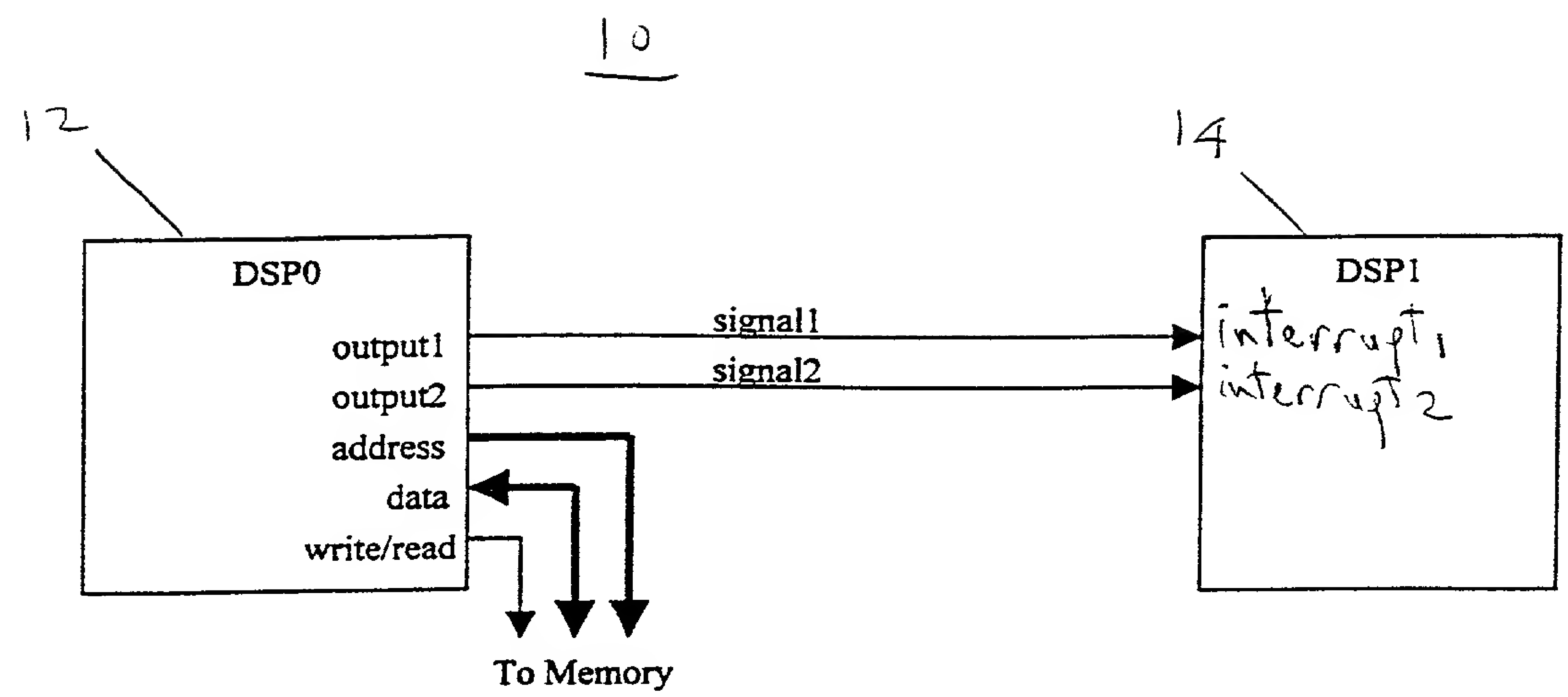


FIG. 1
(prior art)

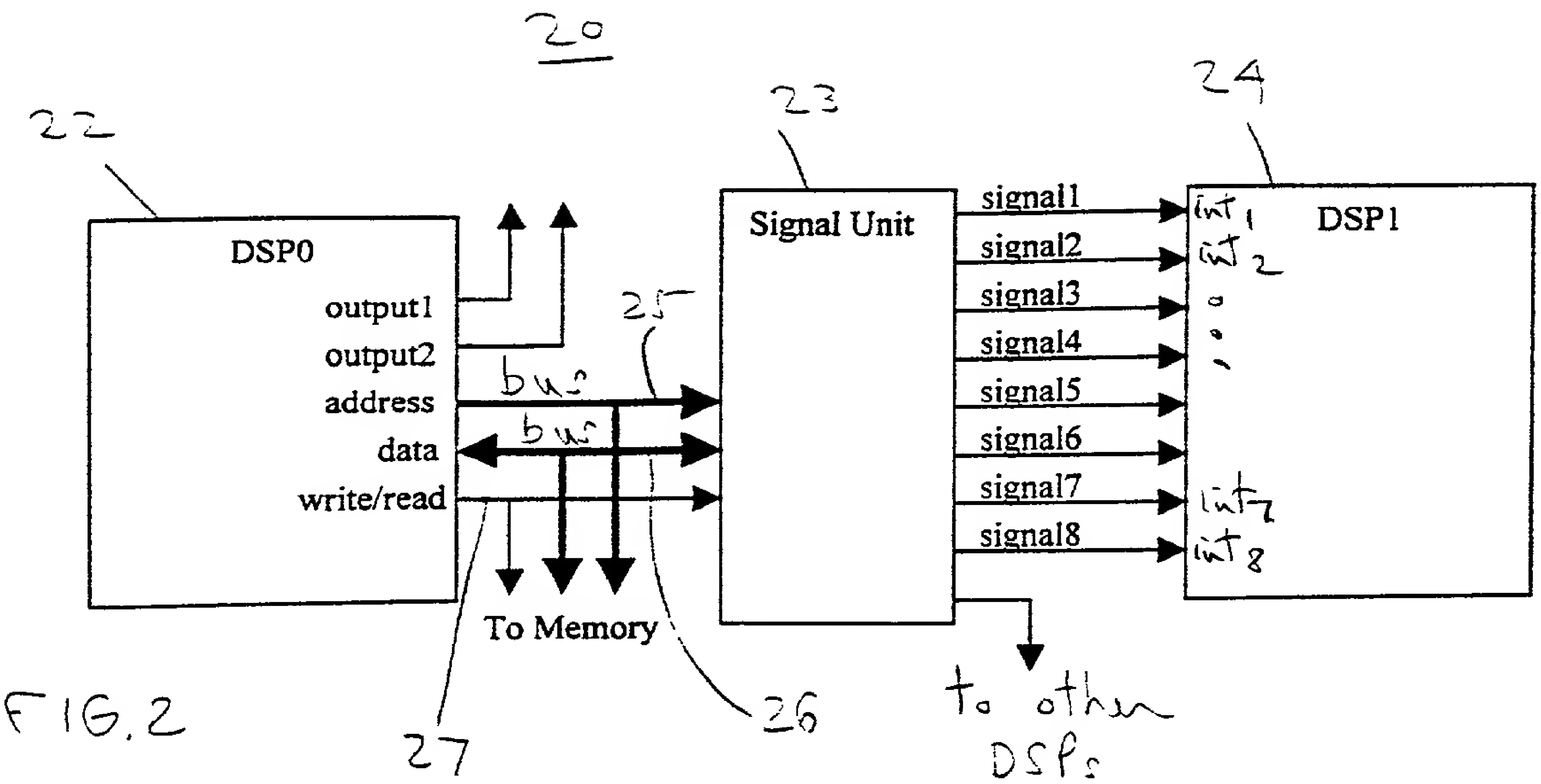

20
22
23
24
DSP0
output1
output2
address
data
write/read
bus
bus
25
Signal Unit
signal1
signal2
signal3
signal4
signal5
signal6
signal7
signal8
DSP1
int1
int2
int7
int8
To Memory
to other DSPs
26
27

FIG. 2

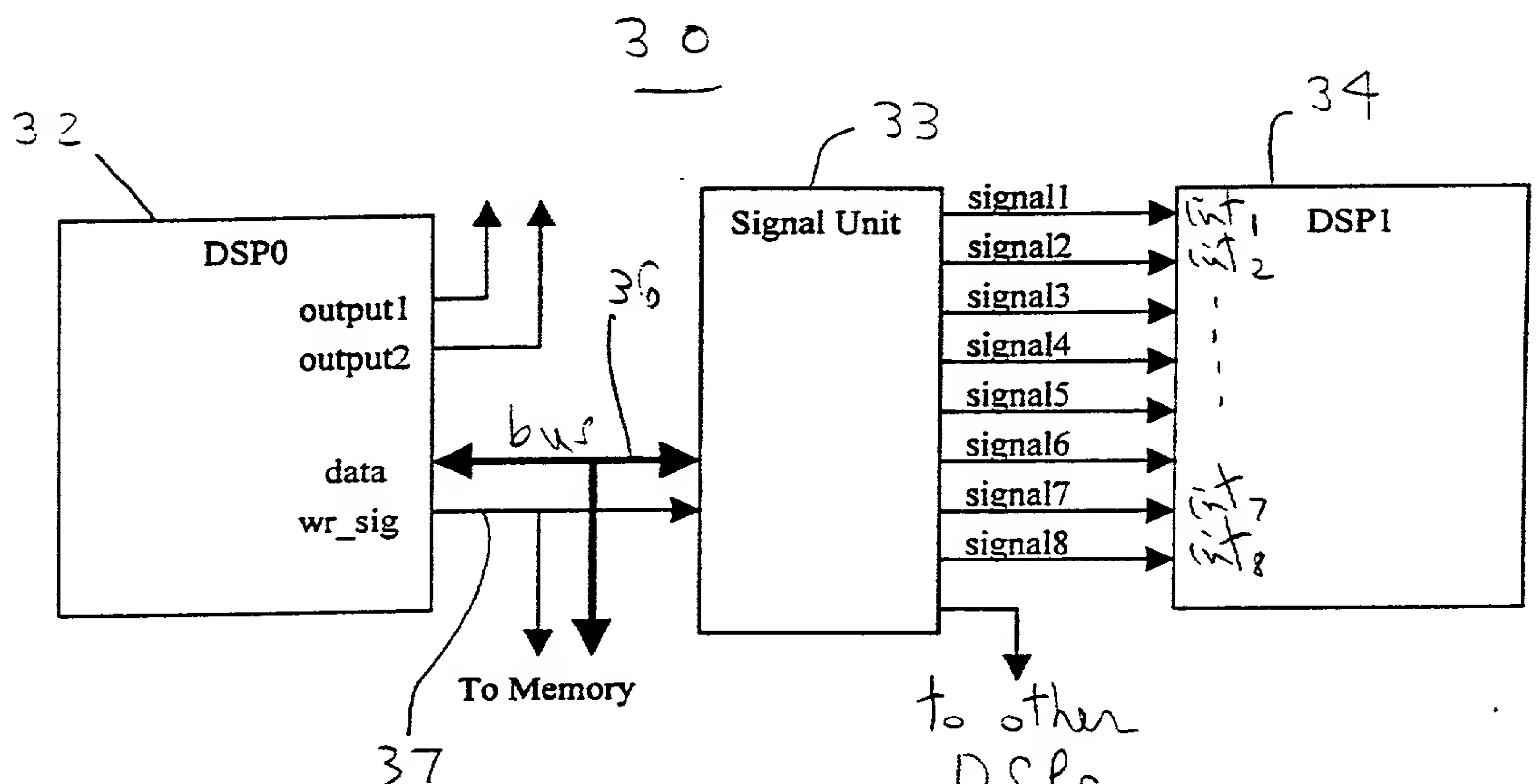
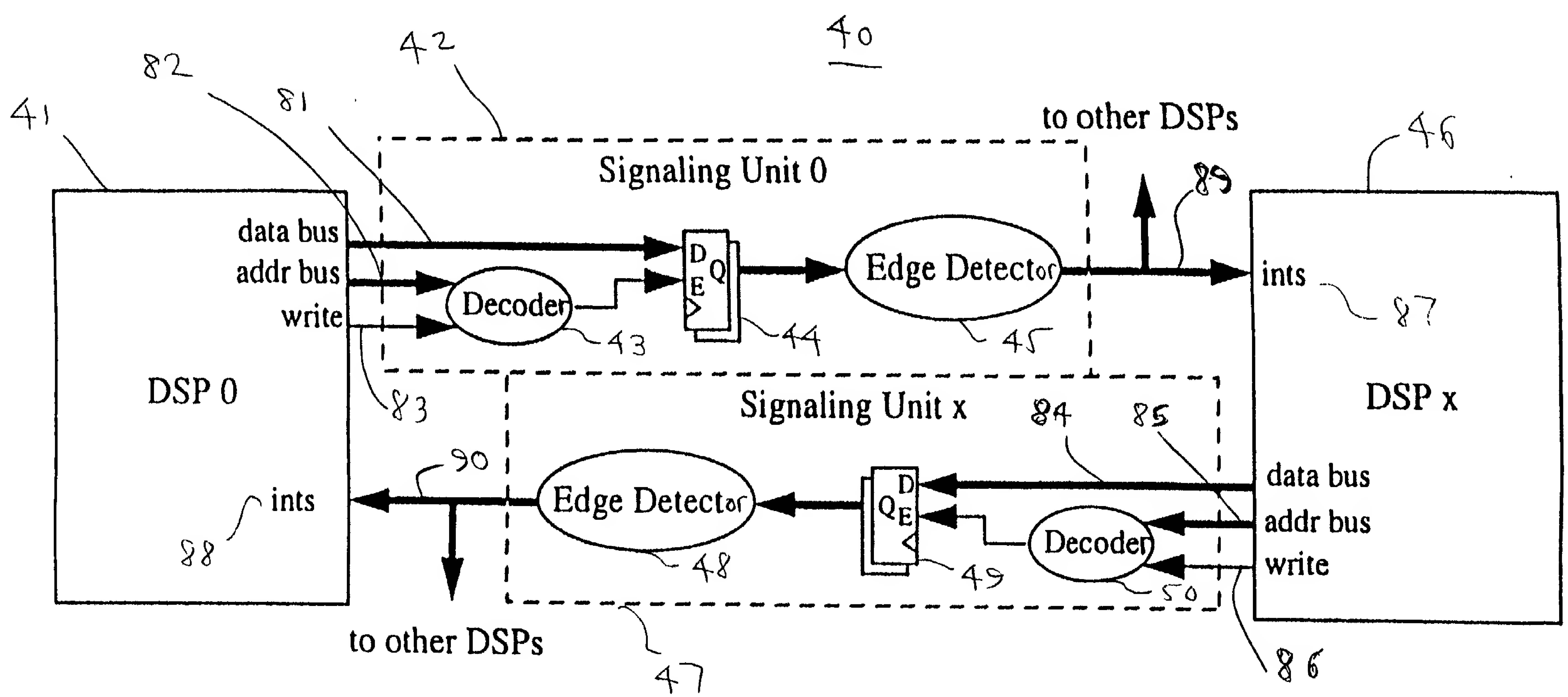

30
32
33
34
DSP0
output1
output2
data
wr_sig
bus
36
Signal Unit
signal1
signal2
signal3
signal4
signal5
signal6
signal7
signal8
DSP1
int1
int2
int7
int8
To Memory
to other DSPs
37

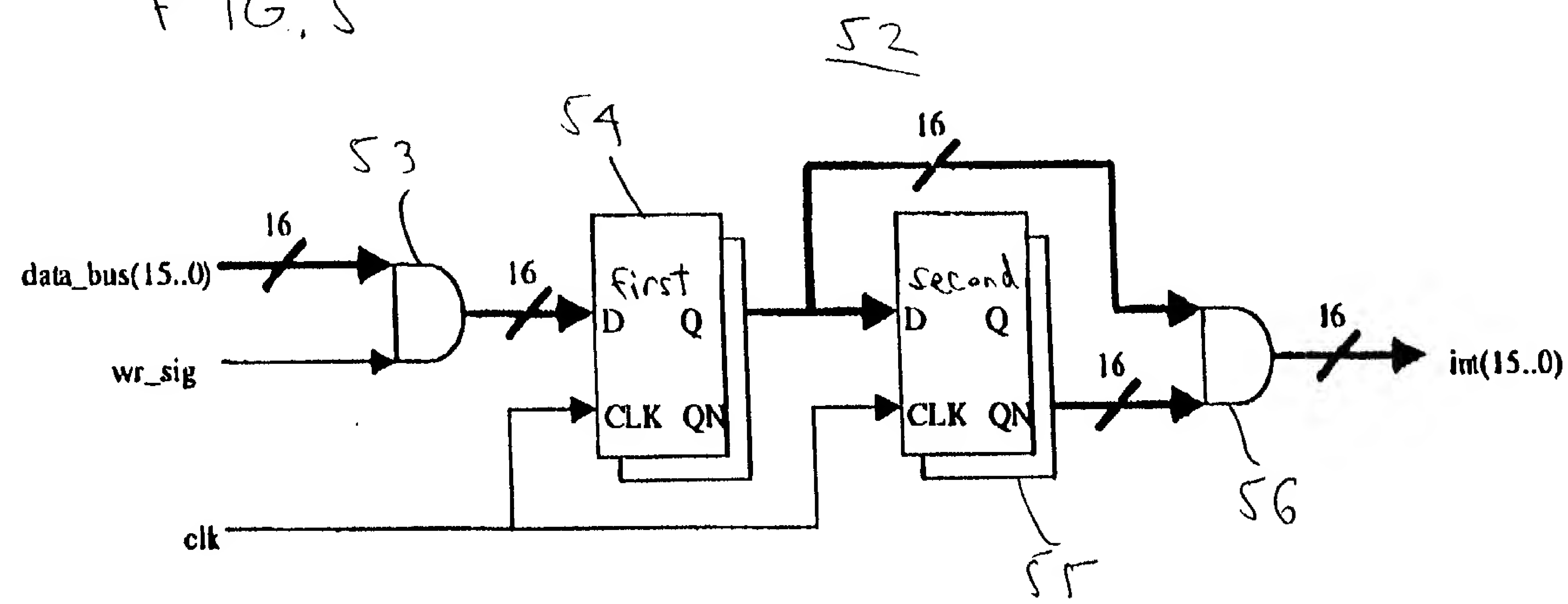
FIG. 3

FIG. 4



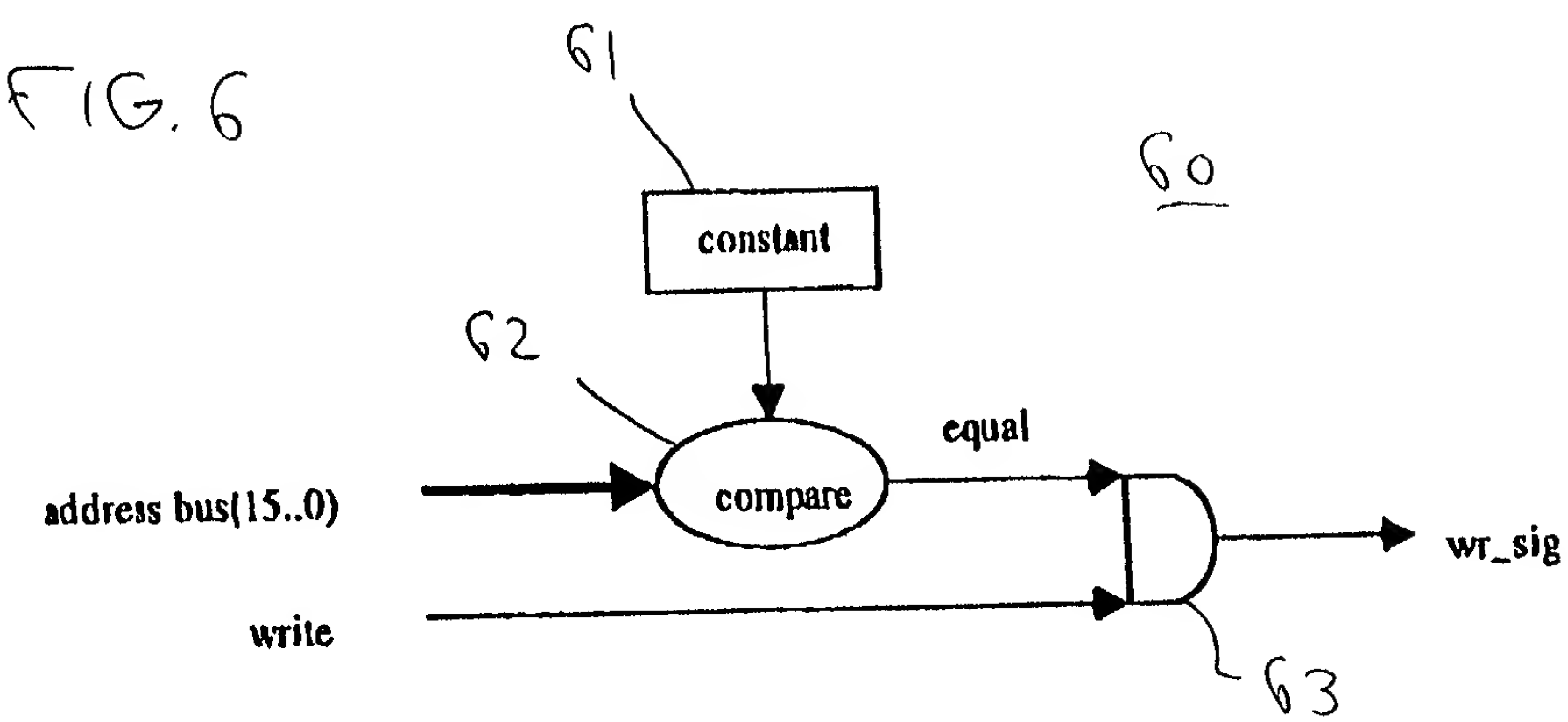
40
41
42
82
81
DSP 0
data bus
addr bus
write
ints
88
83
Signaling Unit 0
Decoder
43
D
E
Q
44
Edge Detector
45
to other DSPs
89
46
DSP x
ints
87
Signaling Unit x
84
85
data bus
addr bus
write
Decoder
50
D
Q
E
49
Edge Detector
48
90
to other DSPs
47
86

FIG. 5



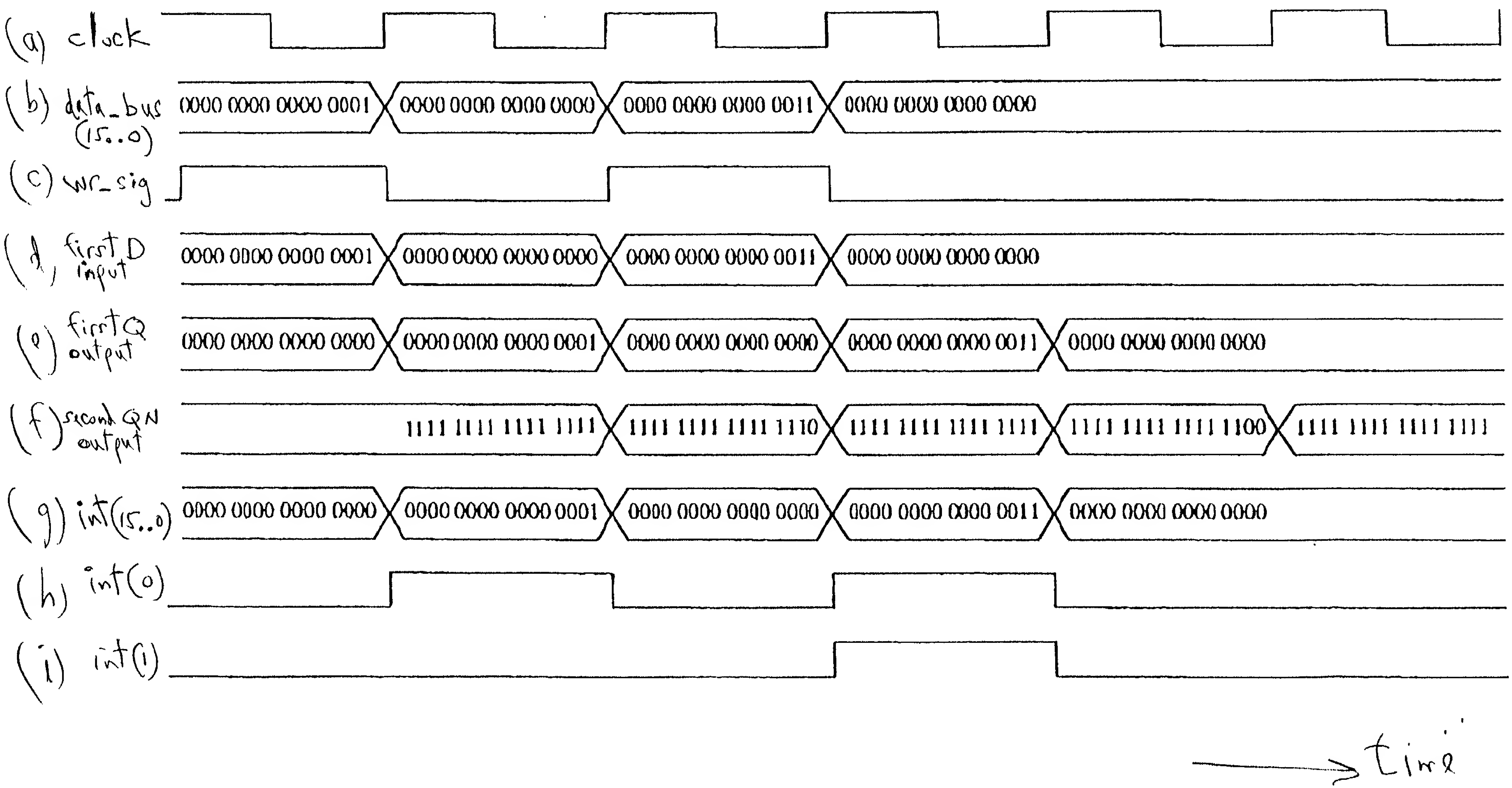
52
53
54
55
56
16
data_bus(15..0)
wr_sig
clk
first
D
Q
CLK
QN
second
int(15..0)

FIG. 6



60
61
62
63
constant
compare
equal
address bus(15..0)
write
wr_sig

FIG. 7


(a) clock
(b) data_bus (15..0)
0000 0000 0000 0001
0000 0000 0000 0000
0000 0000 0000 0011
0000 0000 0000 0000
(c) wr_sig
(d) first D input
0000 0000 0000 0001
0000 0000 0000 0000
0000 0000 0000 0011
0000 0000 0000 0000
(e) first Q output
0000 0000 0000 0000
0000 0000 0000 0001
0000 0000 0000 0000
0000 0000 0000 0011
0000 0000 0000 0000
(f) second QN output
1111 1111 1111 1111
1111 1111 1111 1110
1111 1111 1111 1111
1111 1111 1111 1100
1111 1111 1111 1111
(g) int(15..0)
0000 0000 0000 0000
0000 0000 0000 0001
0000 0000 0000 0000
0000 0000 0000 0011
0000 0000 0000 0000
(h) int(0)
(i) int(1)
time

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Declaration and Power of Attorney

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **INTER-DSP SIGNALING IN A MULTIPLE DSP ENVIRONMENT** the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

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Richard J. Botos	(Reg. No. 32016)
Jeffery J. Brosemer	(Reg. No. 36096)
Kenneth M. Brown	(Reg. No. 37590)
Craig J. Cox	(Reg. No. 39643)
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I hereby appoint the attorney(s) on ATTACHMENT A as associate attorney(s) in the aforementioned application, with full power solely to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected with the prosecution of said application. No other powers are granted to such associate attorney(s) and such associate attorney(s) are specifically denied any power of substitution or revocation.

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ATTACHMENT A

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